ABSTRACT OF THE DISCLOSURE

An integrated circuit testing apparatus having at least two of a first test circuit producing a signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within the integrated circuit; a second test circuit producing a signal for determining at least one of a cross-talk effect on the plurality of components and the accuracy of an interconnect capacitance extraction value; a third test circuit producing a signal for determining at least one of an effect of system noise on the operational speed of the plurality of components and a maximum degradation expected for a logic path between the plurality of components; and a fourth test circuit producing a signal for determining an effect of power supply noise on a signal propagation delay within the plurality of components.